STS3C2F100

N-CHANNEL 100V - 0.110 Ω - 3A SO-8
P-CHANNEL 100V - 0.320 Ω - 1.5A SO-8
COMPLEMENTARY PAIR STripFET™ POWER MOSFET

| TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS3C2F100(N-Channel)	100 V	< 0.145Ω	3.0 A
STS3C2F100(P-Channel)	100 V	< 0.380Ω	1.5 A

- TYPICAL R_{DS}(on) (N-Channel) = 0.110 Ω
- TYPICAL R_{DS}(on) (P-Channel) = 0.320 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- ULTRA LOW GATE CHARGE
- ULTRA LOW ON-RESISTANCE

DESCRIPTION

This MOSFET is the second generation of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC MOTOR DRIVES
- AUDIO AMPLIFIER
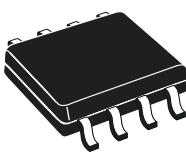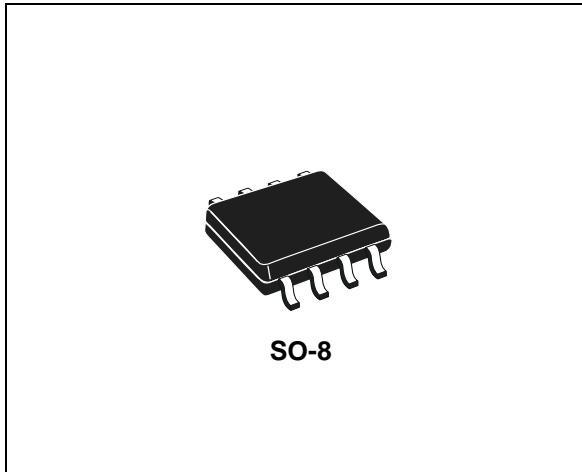
SO-8

INTERNAL SCHEMATIC DIAGRAM
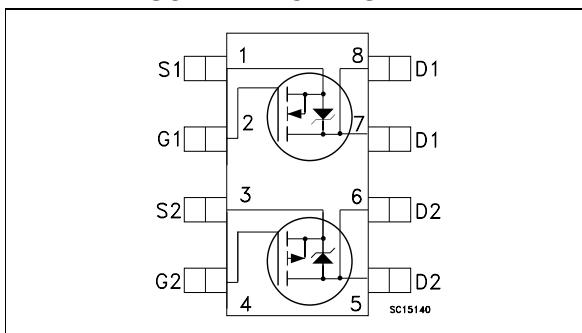
Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STS3C2F100	S3C2F100	SO-8	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	N-CHANNEL	P-CHANNEL	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	100		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	100		V
V_{GS}	Gate- source Voltage	± 20		V
I_D	Drain Current (continuous) at T_C = 25°C	3.0	1.5	A
I_D	Drain Current (continuous) at T_C = 100°C	1.9	1.0	A
I_{DM}(•)	Drain Current (pulsed)	12	6	A
P_{tot}	Total Dissipation at T_C = 25°C	2		W
T_{stg}	Storage Temperature	-55 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

(•) Pulse width limited by safe operating area.

Note: P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

TAB.1 THERMAL DATA

Rthj-amb(1)	Thermal Resistance Junction-ambient	62.5	°C/W

(1) when mounted on 1 in^2 pad of 2 oz. copper, t $\leq$ 10sec.

ELECTRICAL CHARACTERISTICS (T_j = 25 °C unless otherwise specified)

TAB.2 OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	n-ch p-ch	100			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C	n-ch p-ch			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V	n-ch p-ch			±100	nA

TAB.3 ON

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	n-ch p-ch	2 2			V V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 1.5 A V_{GS} = 10 V I_D = 1.0 A	n-ch p-ch		0.110 0.320	0.145 0.380	Ω Ω

TAB.4 DYNAMIC

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} = 20 V I_D= 1.5 A V_{DS} = 30 V I_D= 1.0 A	n-ch p-ch		3 4		S S
C_{iss}	Input Capacitance		n-ch p-ch		460 705		pF pF
C_{oss}	Output Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0	n-ch p-ch		70 83		pF pF
C_{rss}	Reverse Transfer Capacitance		n-ch p-ch		30 30		pF pF

ELECTRICAL CHARACTERISTICS (continued)

TAB.5 SWITCHING ON

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	**N-CHANNEL** V_{DD} = 50 V I_D = 1.5 A R_G = 4.7 Ω V_{GS} = 10 V	n-ch p-ch		16 14		ns ns
t_r	Rise Time	**P-CHANNEL** V_{DD} = 50 V I_D = 1.5 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 1)	n-ch p-ch		25 20		ns ns
Q_g	Total Gate Charge	**N-CHANNEL** V_{DD}=80V I_D=3A V_{GS}=10V	n-ch p-ch		15 20	20 27	nC nC
Q_{gs}	Gate-Source Charge	**P-CHANNEL** V_{DD} = 80V I_D = 1.5A V_{GS}= 10V (see test circuit, Figure 2)	n-ch p-ch		3.7 2.0		nC nC
Q_{gd}	Gate-Drain Charge		n-ch p-ch		4.7 6.0		nC nC

TAB.6 SWITCHING OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	**N-CHANNEL** V_{DD} = 50 V I_D = 1.5 A R_G = 4.7 Ω V_{GS} = 10 V	n-ch p-ch		32 33		ns ns
t_f	Fall Time	**P-CHANNEL** V_{DD} = 50 V I_D = 1.5 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 1)	n-ch p-ch		20 7.5		ns ns

TAB.7 SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current		n-ch p-ch			3.0 1.5	A A
I_{SDM} (•)	Source-drain Current (pulsed)		n-ch p-ch			12 6.0	A A
V_{SD}(∗)	Forward On Voltage	I_{SD} = 3 A V_{GS} = 0 I_{SD} = 1.5 A V_{GS} = 0	n-ch p-ch			1.2 1.2	V V
t_{rr}	Reverse Recovery Time	**N-CHANNEL** I_{SD} = 3 A di/dt = 100A/µs V_{DD} = 50 V T_j =150 °C	n-ch p-ch		90 65		ns ns
Q_{rr}	Reverse Recovery Charge	**P-CHANNEL** I_{SD} = 1.5 A di/dt = 100A/µs V_{DD} = 50 V T_j =150 °C (see test circuit, Figure 3)	n-ch p-ch		230 175		nC nC
I_{RRM}	Reverse Recovery Current		n-ch p-ch		5.0 5.4		A A

(∗) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•) Pulse width limited by safe operating area.

Safe Operating Area n-ch

MC00010

$I_D(A)$

$R_{DS(on)}$LIMITS

10ms
100ms
1s

$T_{JMAX}=175°C$
$T_C=25°C$
SINGLE PULSE

$V_{DS}(V)$

Thermal Impedance n-ch

GC97590

K

d=0.5
0.2
0.1
0.05
0.02
0.01

$Z_{th} = k\ R_{thJ-c}$
$\delta = t_p/\tau$

SINGLE PULSE

$t_p(s)$

Output Characteristics n-ch

GC95660

$I_D(A)$

$V_{GS}=10V$
6V
5V
4V

$V_{DS}(V)$

Transfer Characteristics n-ch

GC95670

$I_D(A)$

$V_{DS}=15V$

$V_{GS}(V)$
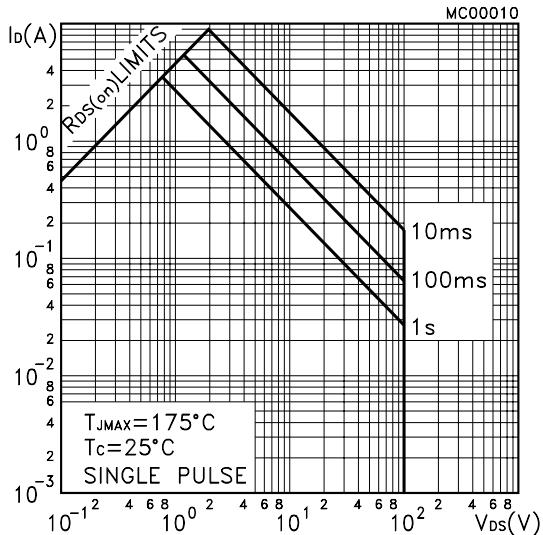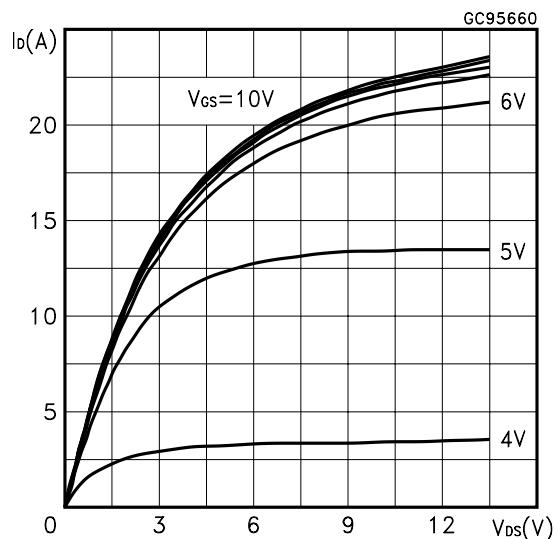
Transconductance n-ch

GC95680

$g_{fs}(S)$

$V_{DS}=20V$

$T_J=-40°C$
25°C
150°C

$I_D(A)$
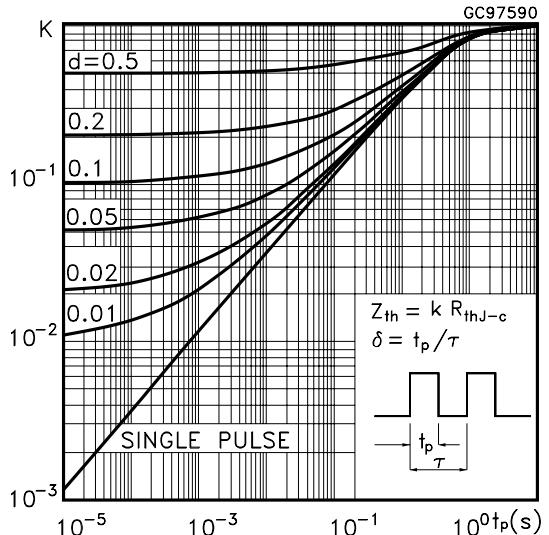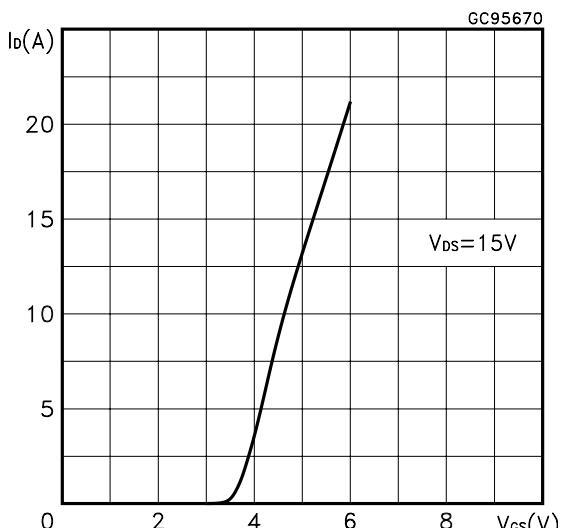
Static Drain-source On Resistance n-ch

GC95690

$R_{DS(on)}$ (Ω)

$V_{GS}=10V$

$I_D(A)$
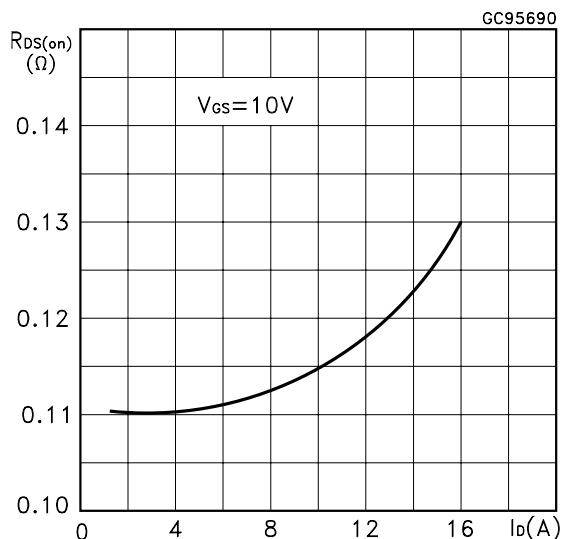
Gate Charge vs Gate-source Voltage **n-ch**
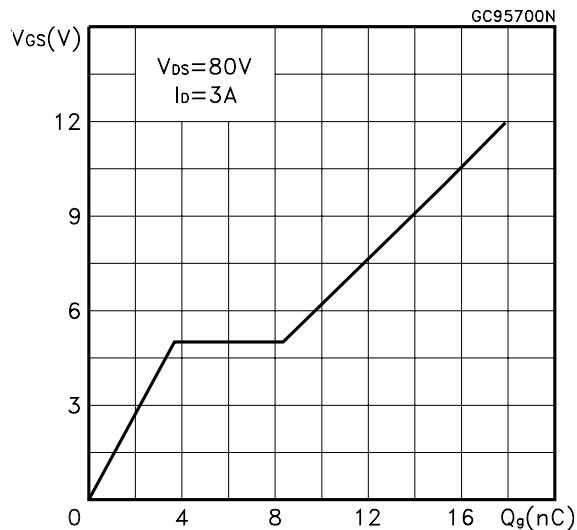
Capacitance Variations **n-ch**
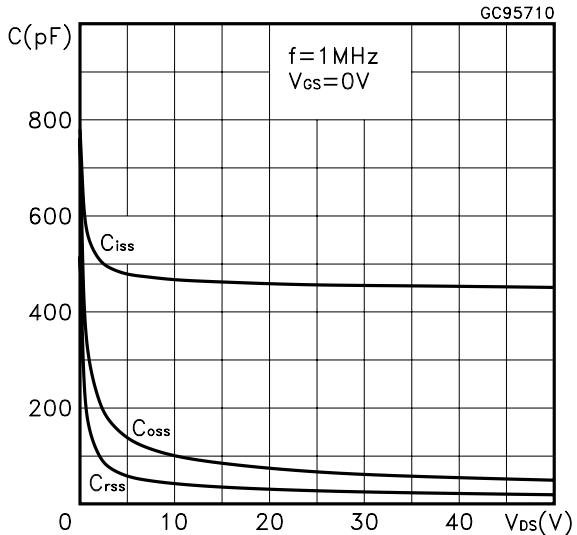
Normalized Gate Threshold Voltage vs Temperature **n-ch**
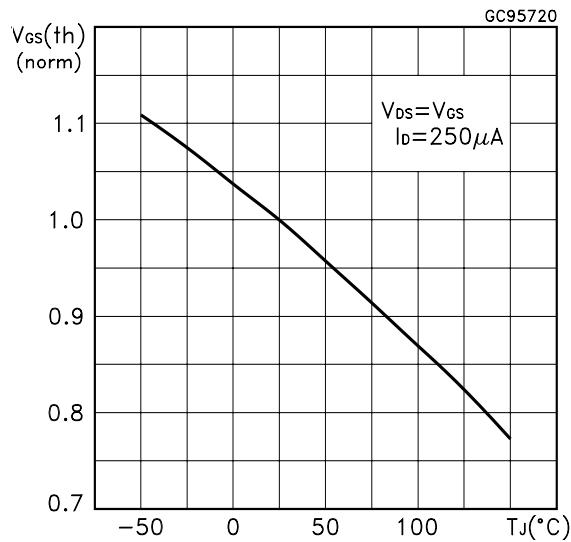
Normalized on Resistance vs Temperature **n-ch**
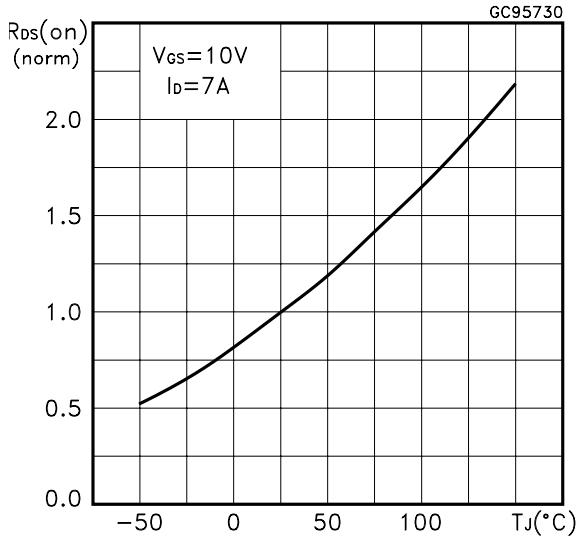
Source-drain Diode Forward Characteristics **n-ch**
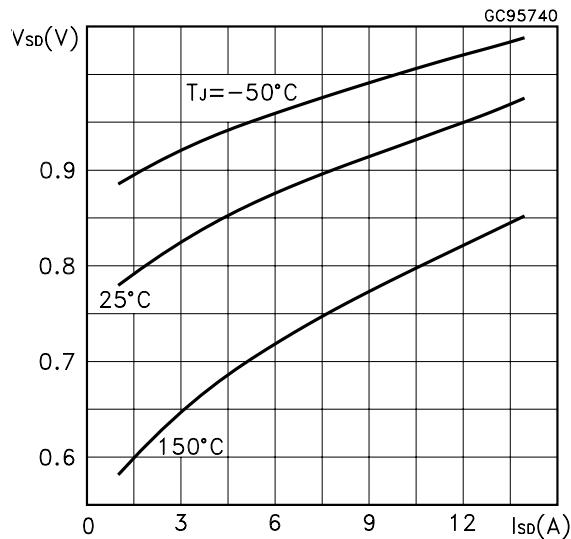


Normalized Breakdown Voltage vs Temperature **n-ch**
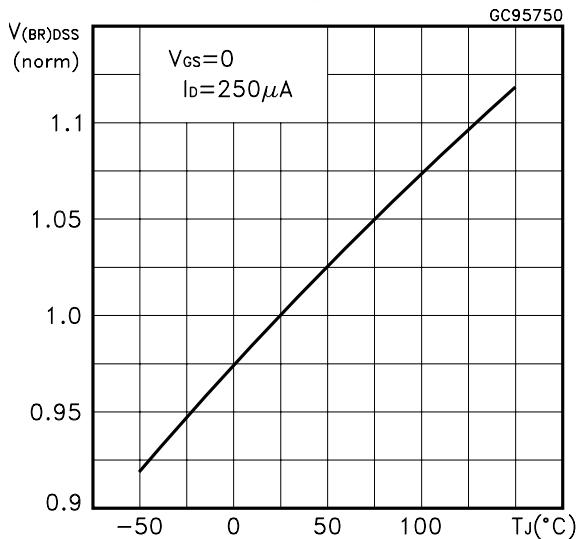
Safe Operating Area **p-ch**
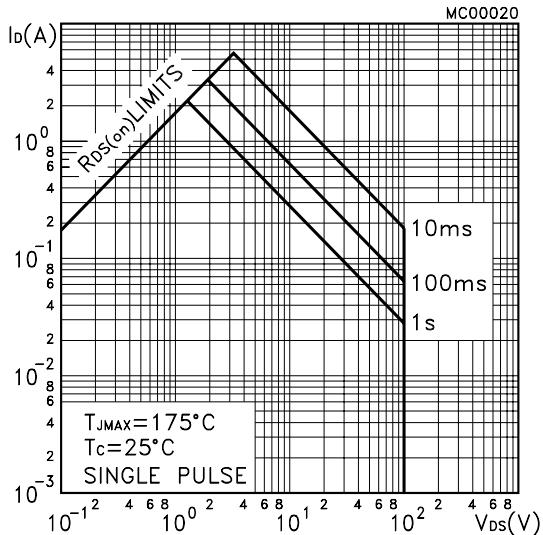
Thermal Impedance **p-ch**
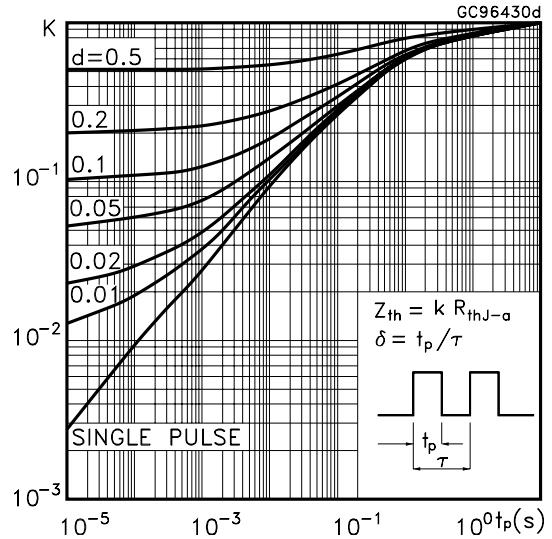
Output Characteristics **p-ch**
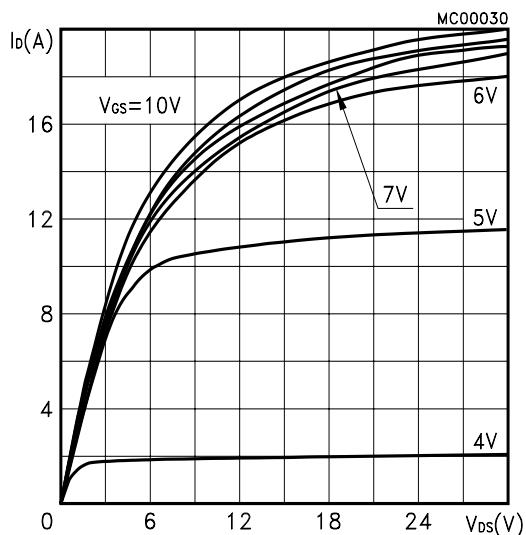
Transfer Characteristics **p-ch**
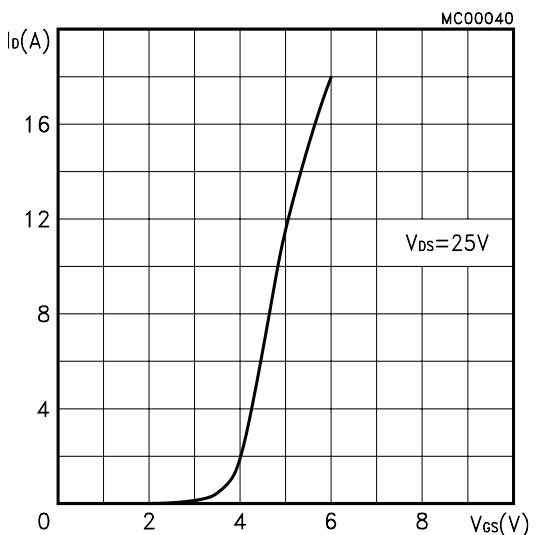
Transconductance **p-ch**
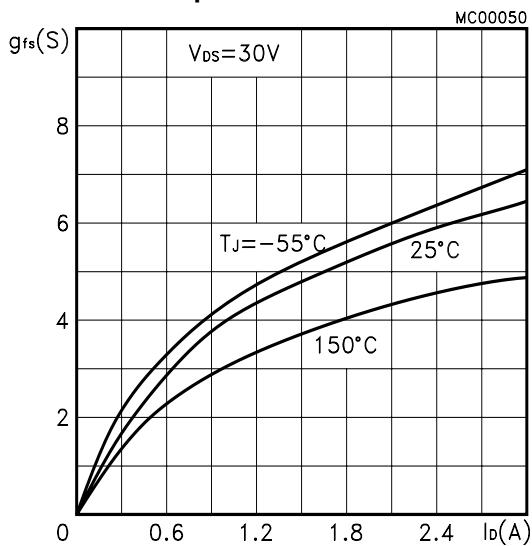
Static Drain-source On Resistance **p-ch**

Gate Charge vs Gate-source Voltage p-ch

MC00070

$V_{GS}(V)$

$V_{DS}=80V$
$I_D=1.5A$

−12

−9

−6

−3

0   6   12   18   24 $Q_g(nC)$

Capacitance Variations p-ch

MC00080

$C(pF)$

$f=1MHz$
$V_{GS}=0V$

1600

1200

800   C_{iss}

400

C_{rss} C_{oss}

0   10   20   30   40 $V_{DS}(V)$

Normalized Gate Threshold Voltage vs Temperature p-ch

MC00090

$V_{GS}(th)$ (norm)

$V_{DS}=V_{GS}$
$I_D=250\mu A$

1.1

1.0

0.9

0.8

0.7

−50   0   50   100 $T_J(°C)$

Normalized on Resistance vs Temperature p-ch

MC00100

$R_{DS}(on)$ (norm)

$V_{GS}=10V$
$I_D=1.5A$

2.8

2.2

1.6

1.0

0.4

−50   0   50   100 $T_J(°C)$

Source-drain Diode Forward Characteristics p-ch

MC00110

$V_{SD}(V)$

$T_J=-55°C$

1.2

0.9

25°C

0.6   150°C

0.3

0   0.6   1.2   1.8   2.4 $I_{SD}(A)$

Normalized Breakdown Voltage vs Temperature p-ch

MC00120

$V_{(BR)DSS}$ (norm)

$V_{GS}=0$
$I_D=1mA$

1.2

1.1

1.0

0.9

0.8

−50   0   50   100 $T_J(°C)$
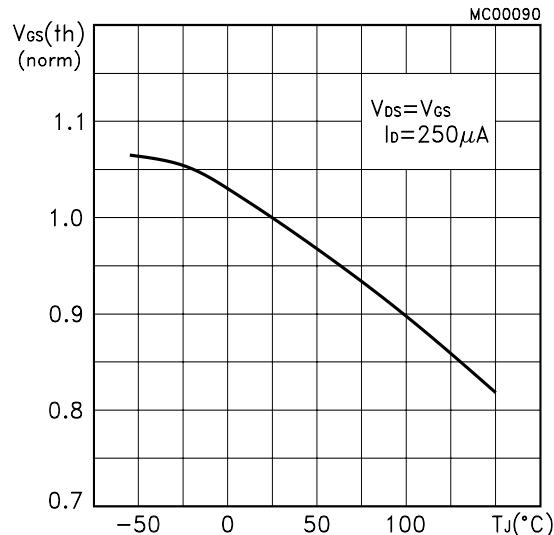
**Fig. 1:** Switching Times Test Circuits For Resistive Load
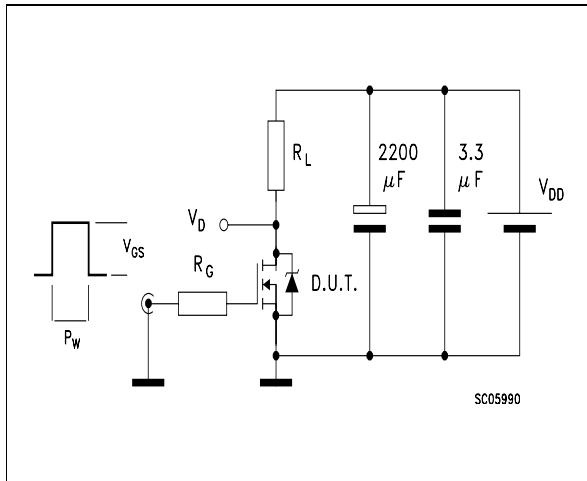

Fig. 2: Gate Charge test Circuit
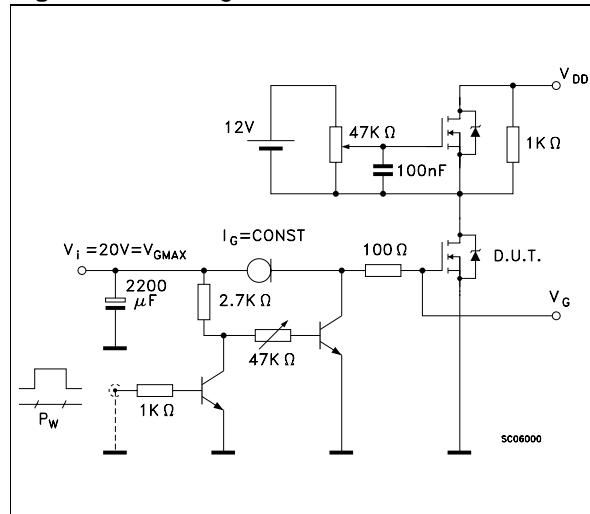
Fig. 3: Test Circuit For Diode Recovery Behaviour
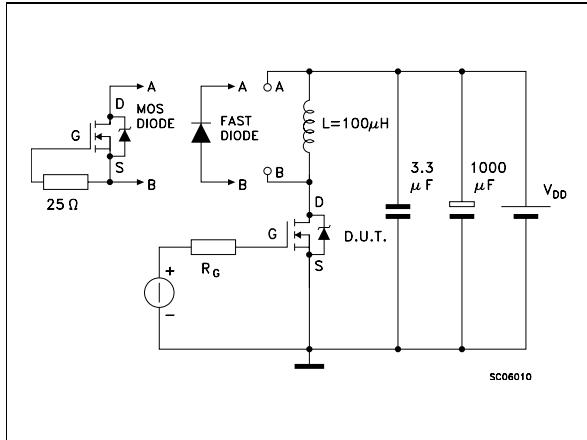
SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					
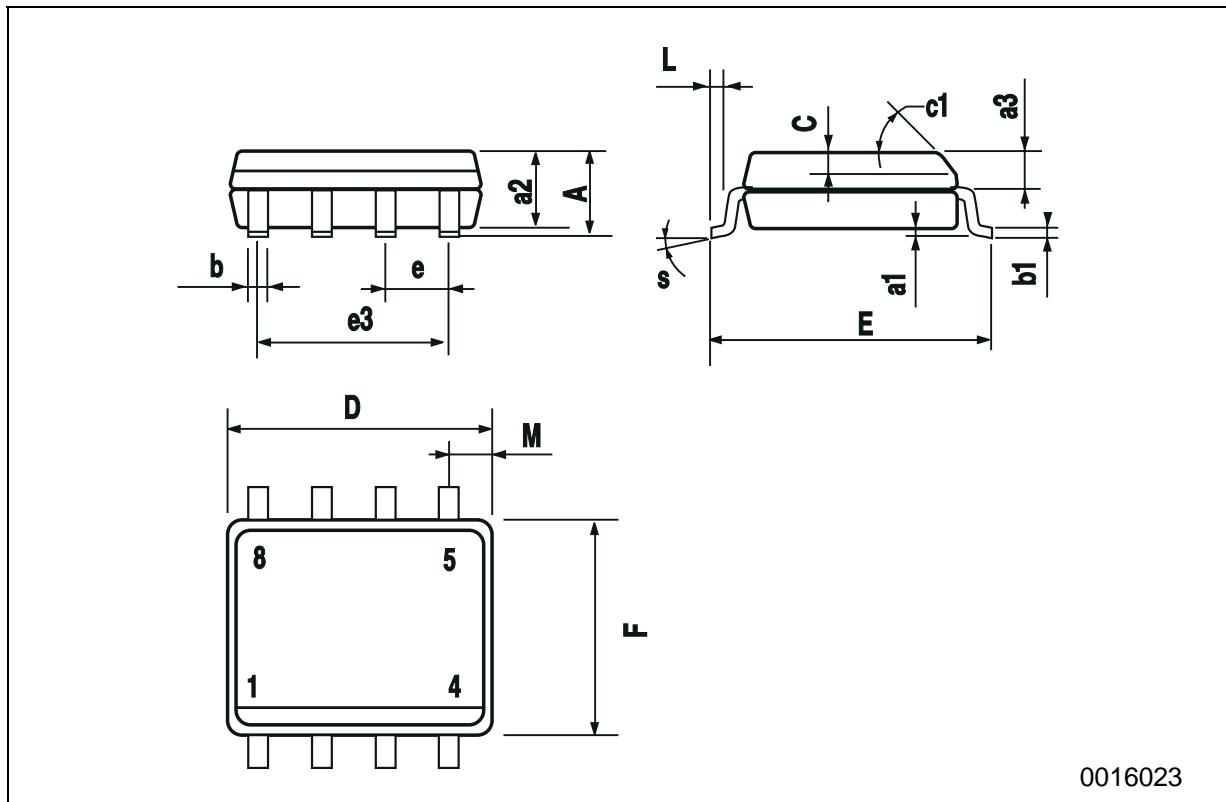
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Revision History

Date	Revision	Description of Changes
Friday 18 June 2004	1.0.1	FIRST ISSUE

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